Abstract of the Disclosure

The present invention provides an apparatus for designing a semiconductor integrated circuit, which is capable of satisfying timing constraints without providing BFBs, and improving a convergent property at optimization, and a design method therefor. An LSI automatic design simulator (10) determines the number of clocks employed in a clock generating functional part (30) and delays in respective clocks, allocates the clocks set as clock systems, and verifies constraint conditions with respect to design, based on the respective clocks. A tree determining functional part (32) adjusts skews of the respective clocks through the use of the produced cock systems, makes delay adjustments to the clocks, verifies a layout adjustment, and fetches therein data supplied thereto without timing constraint violation, thereby making it possible to further enhance a convergent property that satisfies all of timing constraints.